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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,977	10/07/2003	William R. Dunn	UN11773-012	4778

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EXAMINER	
WANG, GEORGE Y	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,977	DUNN ET AL.	
	Examiner	Art Unit	
	George Y. Wang	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-10,12-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-10,12-14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/04, 3/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on May 25, 2004 and March 31, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 12-14 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohnishi et al. (U.S. Patent No. 6,885,412, hereafter "Ohnishi").

4. As to claim 12, Ohnishi discloses a flat panel display comprising a front glass plate (fig. 3, ref. 2), a rear glass plate (fig. 3, ref. 1), a layer of liquid crystals (fig. 3, ref. 3) interposed between the front and rear glass plates, a TFT array layer (fig. 3, ref. 13) interposed between the front and rear glass plates, and a metal layer integral (fig. 3, ref. 8) to the TFT array layer (col. 12, line 64 – col. 13, line 2).

5. Regarding claims 13-14, Ohnishi discloses the flat panel display device as recited above where the metal heater layer is patterned onto the TFT array layer and is comprised of a grid intersecting horizontal and vertical lines (fig. 3, ref. 11-13; col. 6, lines 6-24).

6. As per claims 18-19, Ohnishi discloses the flat panel display device as recited above further comprising a thermal sensor integral to and applied to the TFT array layer (fig. 2, ref. "temperature detection section"; col. 12, lines 54-63).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 2, 4-9, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi in view of Taniguchi et al. (U.S. Patent No. 6,839,104, hereafter "Taniguchi") and in further view of Shin et al. (U.S. Patent No. 6,417,900, hereafter "Shin").

9. As per claim 5-6 and 16-17, Ohnishi discloses the flat panel display device as recited above, however, the reference fails to specifically disclose a black mask EMI

layer interposed between the glass plates and where the black mask EMI layer is electrically tied to zero potential and isolated from V_{com} and where the metal heater layer is hidden from view behind the black mask EMI layer.

Taniguchi discloses an LCD device having a black mask EMI layer (fig. 20, ref. 6) disposed on the upper glass substrate and is isolated from V_{com} (fig. 20, ref. 24).

Shin discloses an LCD device having a black matrix layer that has a low electrical resistance set to be at ground potential (col. 5, lines 45-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a black mask EMI layer interposed between the glass plates and where the black mask EMI layer is electrically tied to zero potential and isolated from V_{com} and where the metal heater layer is hidden from view behind the black mask EMI layer in the flat panel device of Ohnishi since one would be motivated to prevent light leakage of the light and interface (Taniguchi, col. 2, lines 57-59) as well as obtain a wide-angle viewing display (Shin, col. 9, lines 44-45).

10. Regarding claims 2 and 8, Ohnishi discloses the flat panel display device as recited above further comprising an insulating dielectric layer (fig. 3, ref. 9) interposed between the inside surfaces of the front and glass plates and over-coated onto the metal heater layer (fig. 3, ref. 8).

11. As to claim 4 and 7, Ohnishi discloses the flat panel display device as recited above where the metal heater layer is patterned onto the TFT array layer and is

comprised of a grid intersecting horizontal and vertical lines (fig. 3, ref. 11-13; col. 6, lines 6-24).

12. As per claim 9, Ohnishi discloses the flat panel display device as recited above further comprising a thermal sensor integral to and applied to the TFT array layer (fig. 2, ref. "temperature detection section"; col. 12, lines 54-63).

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi, Taniguchi, and Shin, in view of Muhlemann (U.S. Patent No. 6,774,883).

Ohnishi, when modified by Tanaguchi and Shin, discloses the flat panel display device as recited above, however, the reference fails to specifically disclose that the thermal sensors comprise an array of diodes.

Muhlemann discloses an LCD where the thermal sensors comprise an array of diodes (col. 1, lines 56-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the thermal sensors Ohnishi to comprise an array of diodes since they are well known in the art of displays (col. 1, line 56). Furthermore, one would be motivated to obtain thermal information without resulting in errors in signal propagation, crosstalk, and inaccuracy in the comparator (col. 1, lines 27-30).

14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi in view of Muhlemann.

Ohnishi discloses the flat panel display device as recited above, however, the reference fails to specifically disclose that the thermal sensors comprise an array of diodes.

Muhlemann discloses an LCD where the thermal sensors comprise an array of diodes (col. 1, lines 56-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the thermal sensors Ohnishi to comprise an array of diodes since they are well known in the art of displays (col. 1, line 56). Furthermore, one would be motivated to obtain thermal information without resulting in errors in signal propagation, crosstalk, and inaccuracy in the comparator (col. 1, lines 27-30).

Double Patenting

15. Claims 2, 4-9, 12-14, and 16-19 of this application conflict with claims 1-3, 5-7, and 12 of Application No. 10/769,843. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

gw
June 11, 2005